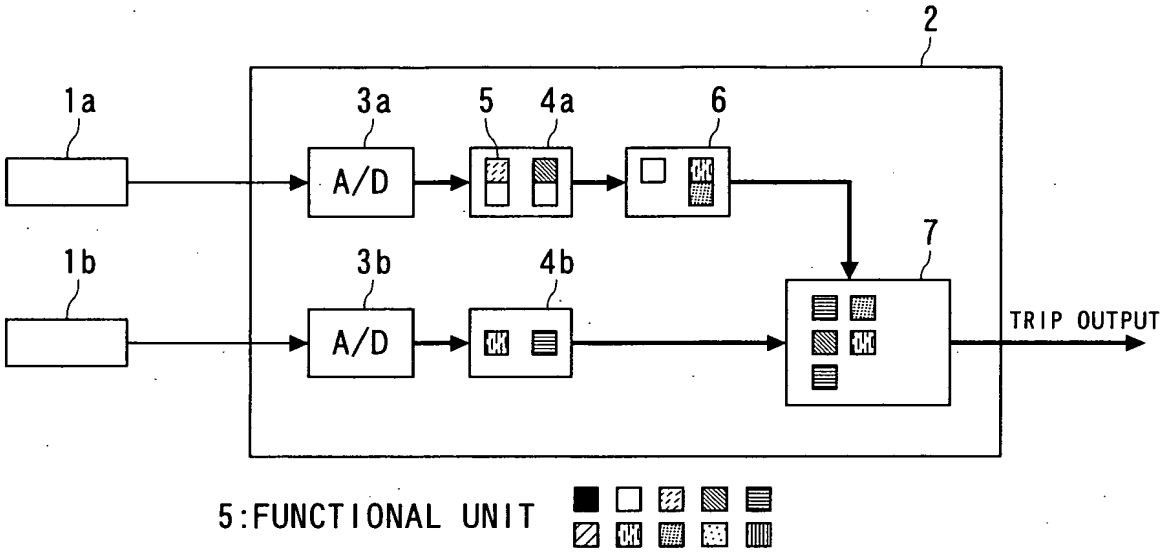
2
1a
3a
5
4a
6
A/D
1b
3b
4b
7
A/D
TRIP OUTPUT
5:FUNCTIONAL UNIT

FIG. 1

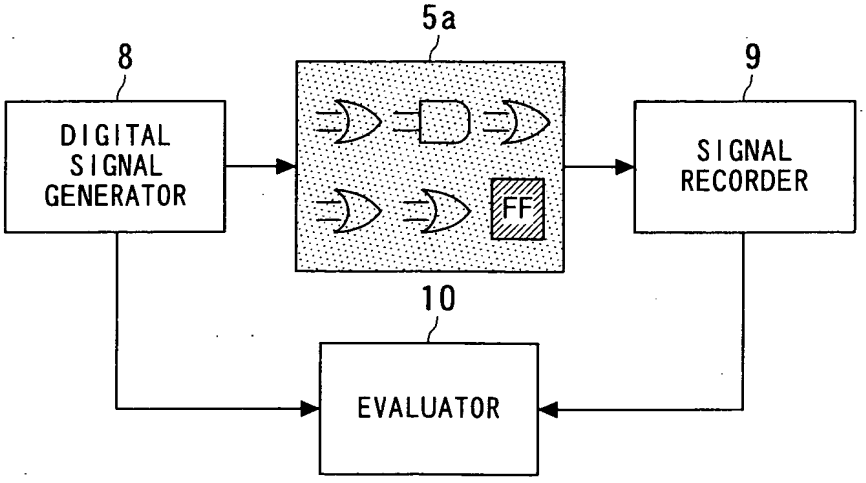
5a
8
9
DIGITAL SIGNAL GENERATOR
FF
SIGNAL RECORDER
10
EVALUATOR

FIG. 2

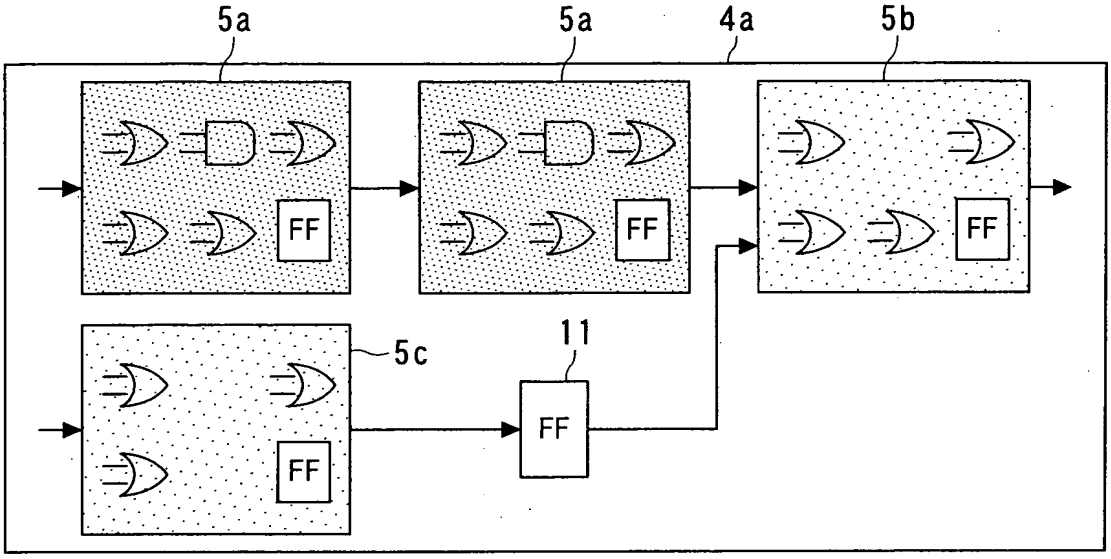
5a
5a
4a
5b
FF
FF
FF
5c
11
FF
FF

FIG. 3

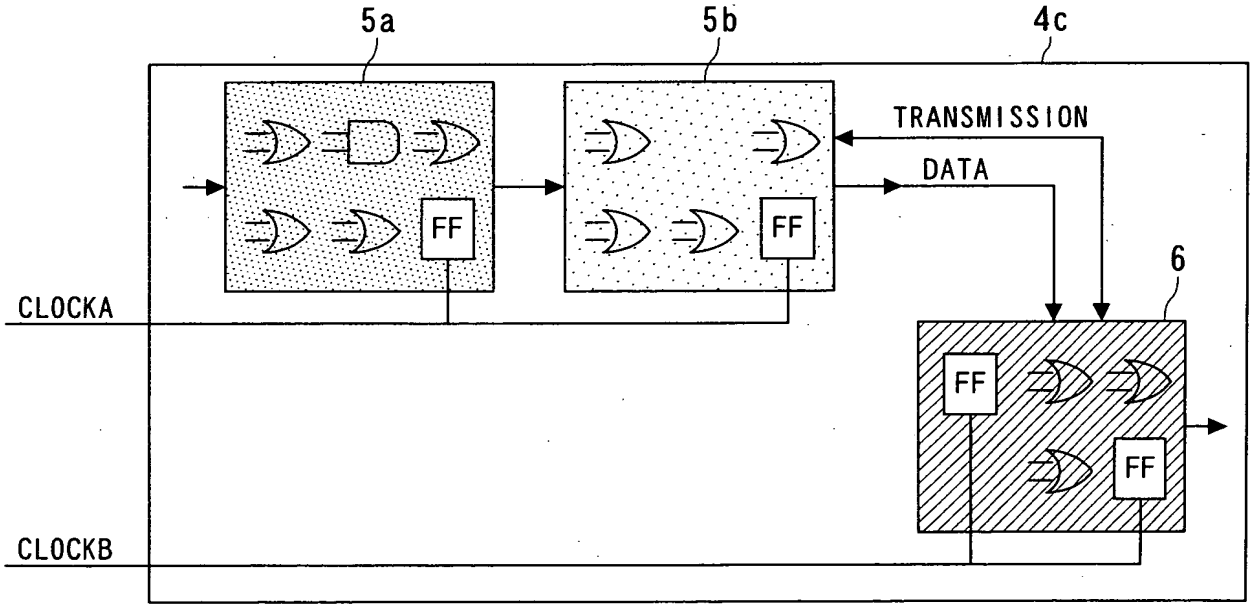
5a
5b
4c
TRANSMISSION
DATA
FF
FF
6
CLOCKA
FF
FF
CLOCKB

FIG. 4

VHDL STATEMENT

```
—Comparator ver0.1

library IEEE;use IEEE.std_logic_1164.all;

entity COMPARATOR is
generic(WIDTH : integer:=4);
port(CLK : in std_logic;
   aclr : in std_logic;
   INP : in std_logic_vector(WIDTH-1 downto 0);
   REF : in std_logic_vector(WIDTH-1 downto 0);
   GT : out std_logic;
   EQ : out std_logic;
   LT : out std_logic);
end COMPARATOR;

architecture RTL of COMPARATOR is
Begin process(CLK,aclr) begin

if(aclr = '0')then
   GT <='0';
   EQ <='0';
   LT <='0';
elsif(CLK'event and CLK='1')then
   if INP>REF then
      GT<='1';EQ<='0';LT<='0';
   elsif INP < REF then
      GT<='0';EQ<='0';LT<='1';
   elsif INP = REF then
      GT<='0';EQ<='1';LT<='0';
   else
      GT<='X';EQ<='X';LT<='X';
   end if;
  end if;
end process;
end RTL;
```

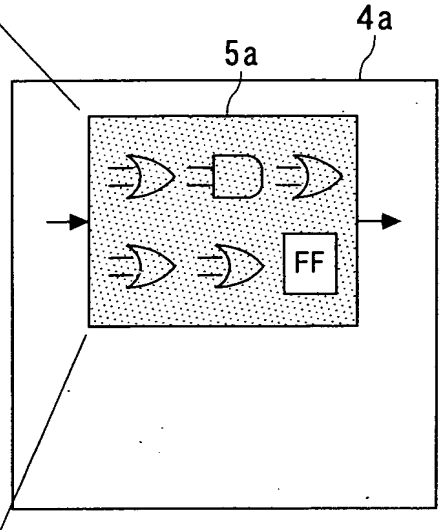

FIG. 5

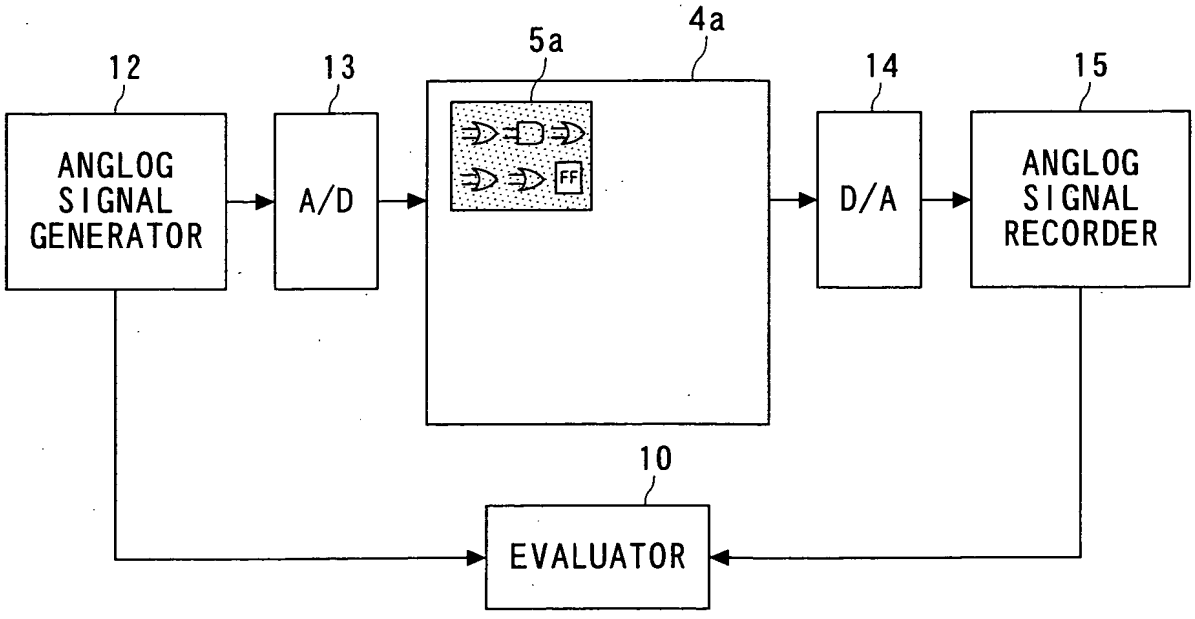

FIG. 6

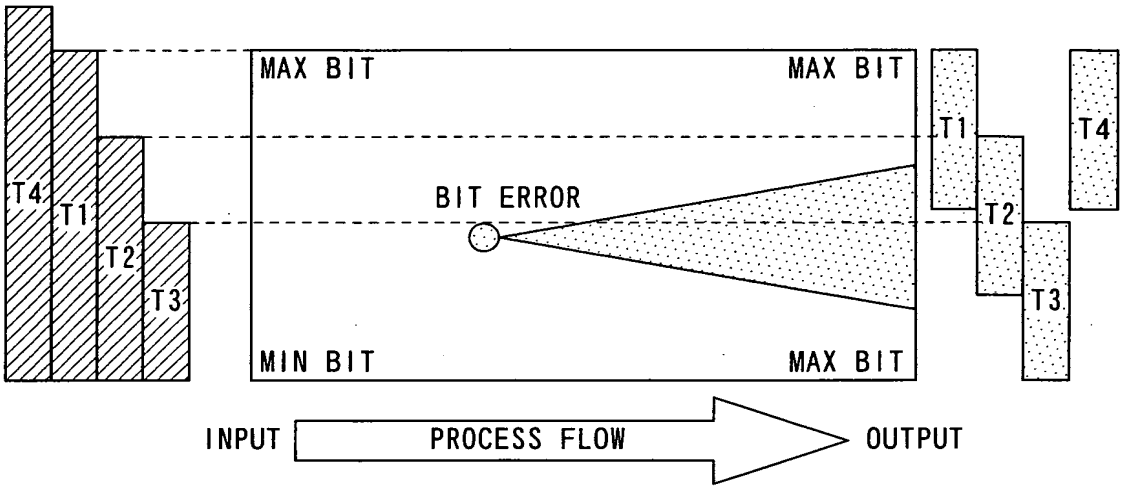
MAX BIT
MAX BIT
T1
T4
T4
T1
T2
T3
BIT ERROR
T2
T3
MIN BIT
MAX BIT
INPUT
PROCESS FLOW
OUTPUT

FIG. 7

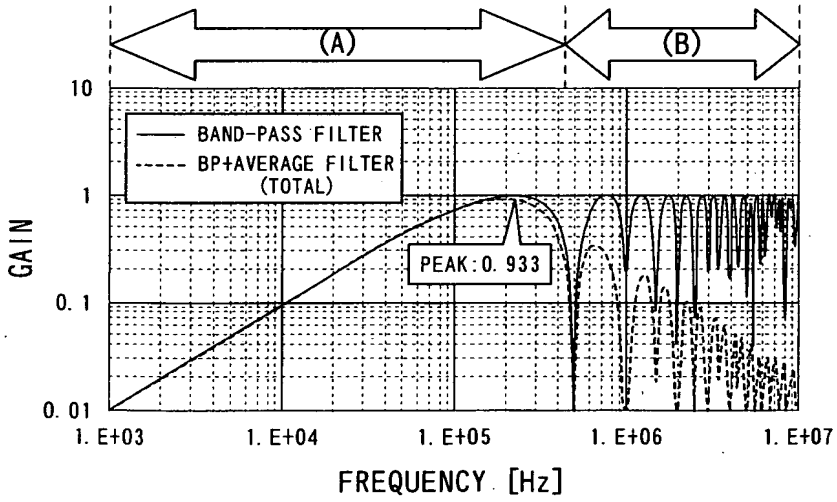
(A)
(B)
10
1
0.1
0.01
BAND-PASS FILTER
BP+AVERAGE FILTER
(TOTAL)
PEAK:0.933
GAIN
1.E+03
1.E+04
1.E+05
1.E+06
1.E+07
FREQUENCY [Hz]

FIG. 8

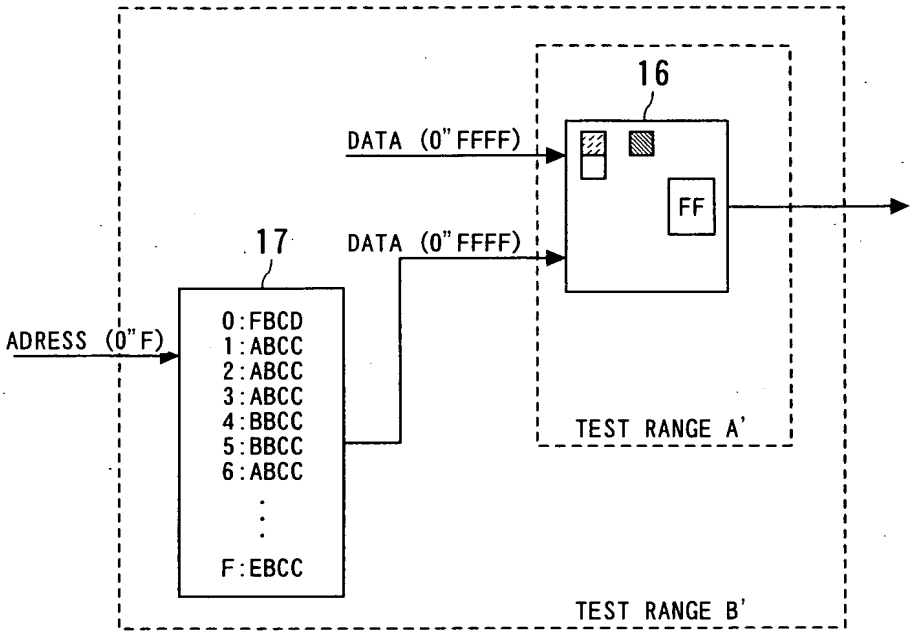
16
DATA (0"FFFF)
FF
17
DATA (0"FFFF)
ADRESS (0"F)
0:FBCD
1:ABCC
2:ABCC
3:ABCC
4:BBCC
5:BBCC
6:ABCC
F:EBCC
TEST RANGE A'
TEST RANGE B'

FIG. 9

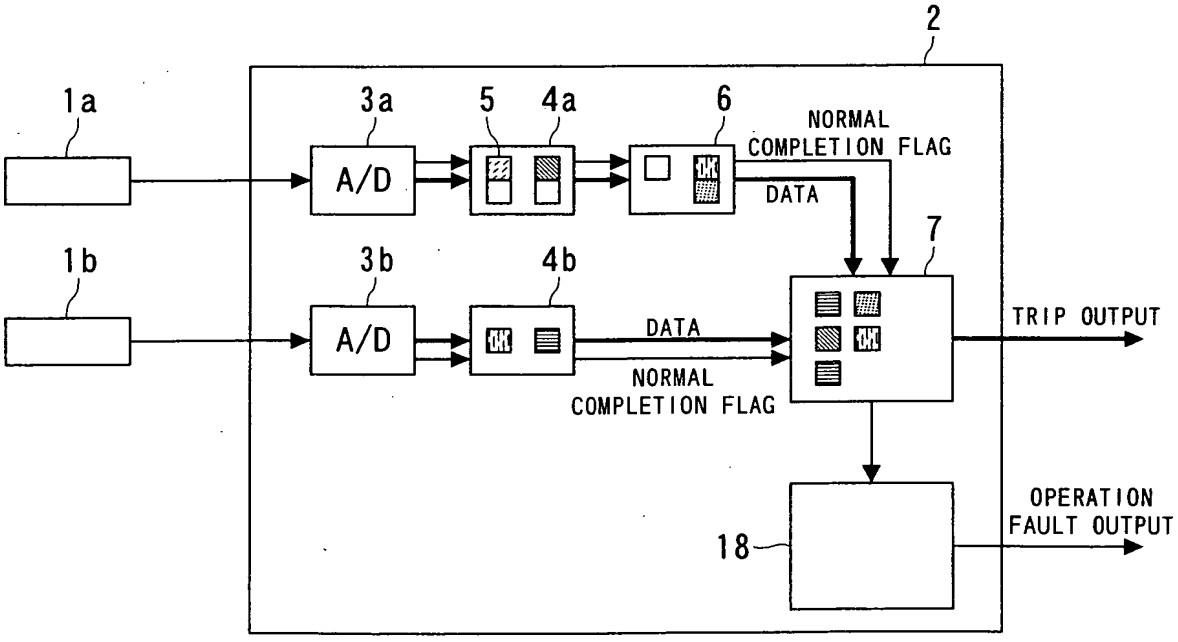
2
1a
3a
5
4a
6
NORMAL
COMPLETION FLAG
A/D
DATA
7
1b
3b
4b
A/D
DATA
NORMAL
COMPLETION FLAG
TRIP OUTPUT
OPERATION
FAULT OUTPUT
18

FIG. 10

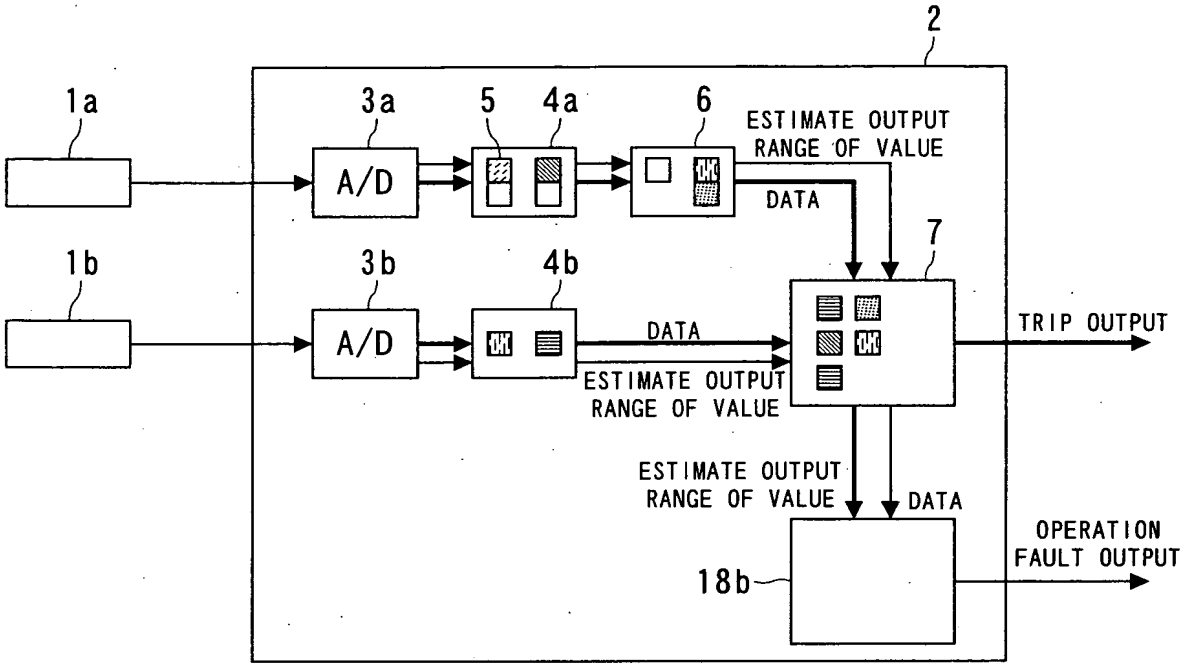
2
1a
3a
5
4a
6
ESTIMATE OUTPUT RANGE OF VALUE
DATA
A/D
1b
3b
4b
7
A/D
DATA
TRIP OUTPUT
ESTIMATE OUTPUT RANGE OF VALUE
ESTIMATE OUTPUT RANGE OF VALUE
DATA
OPERATION FAULT OUTPUT
18b

FIG. 11

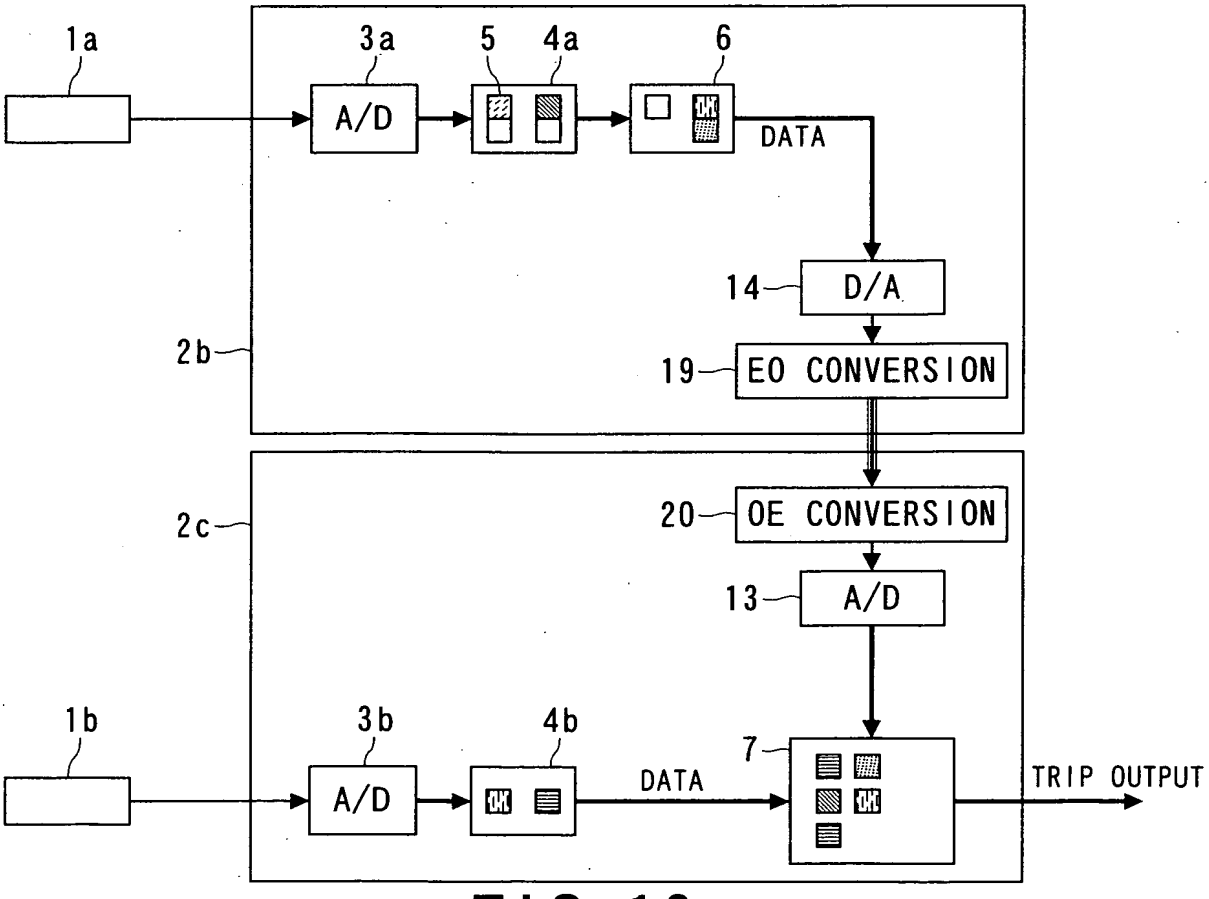
1a
3a
5
4a
6
A/D
DATA
14
D/A
2b
19
EO CONVERSION
2c
20
OE CONVERSION
13
A/D
1b
3b
4b
7
A/D
DATA
TRIP OUTPUT

FIG. 12

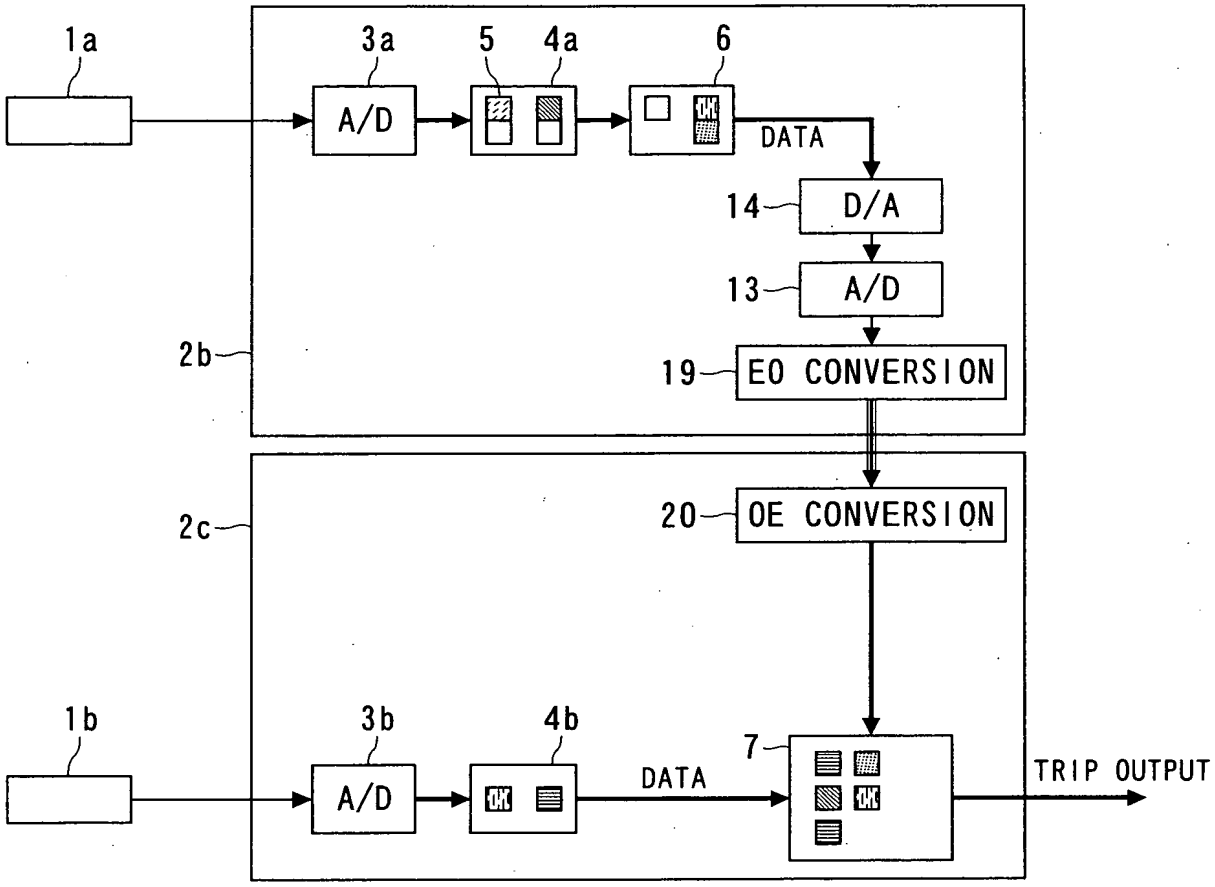
1a
3a
5
4a
6
A/D
DATA
14
D/A
13
A/D
2b
19
EO CONVERSION
2c
20
OE CONVERSION
1b
3b
4b
7
A/D
DATA
TRIP OUTPUT

FIG. 13

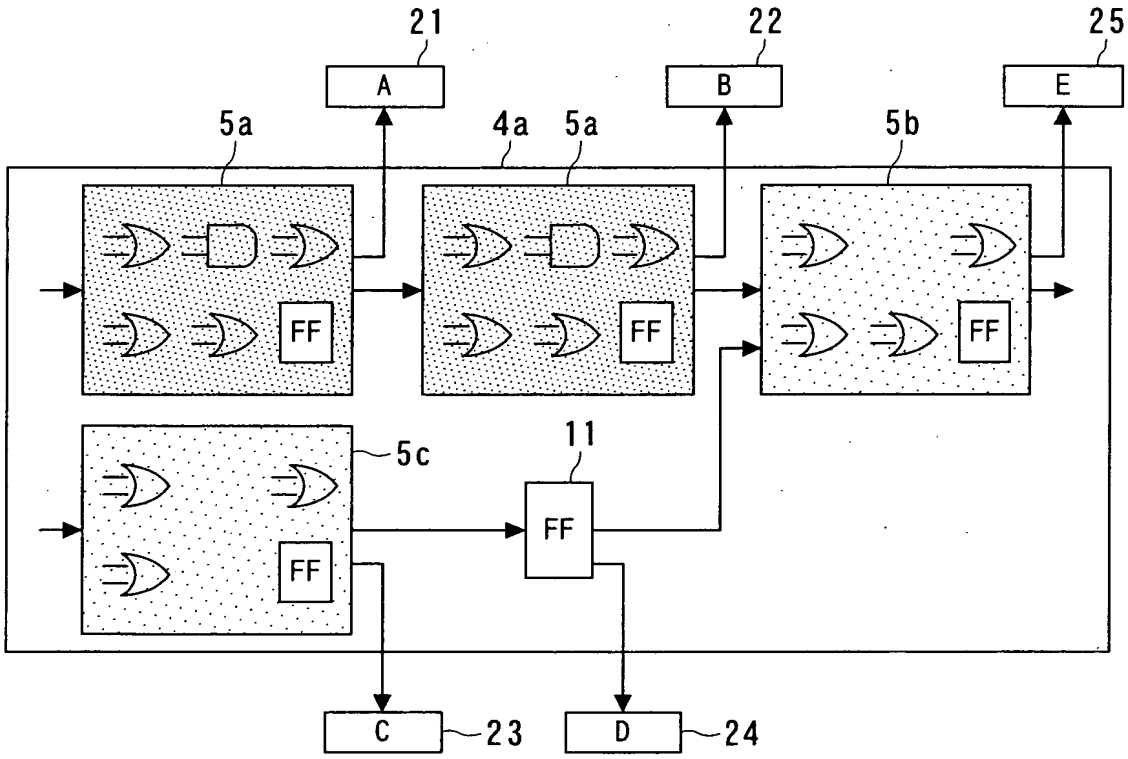

FIG. 14

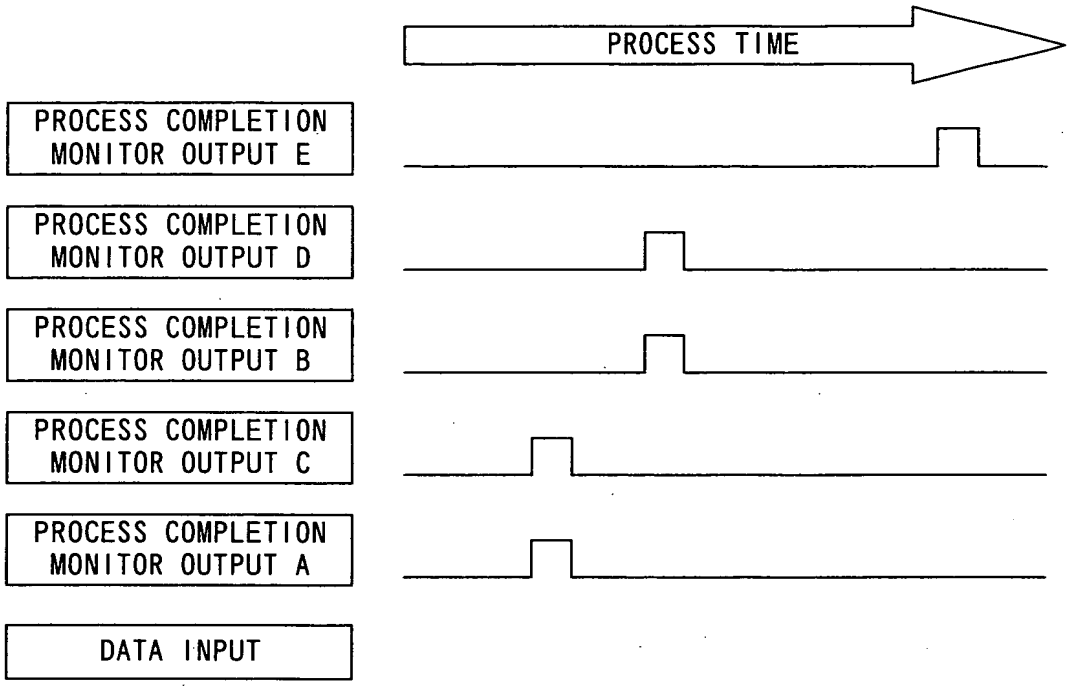
PROCESS TIME
PROCESS COMPLETION MONITOR OUTPUT E
PROCESS COMPLETION MONITOR OUTPUT D
PROCESS COMPLETION MONITOR OUTPUT B
PROCESS COMPLETION MONITOR OUTPUT C
PROCESS COMPLETION MONITOR OUTPUT A
DATA INPUT

FIG. 15

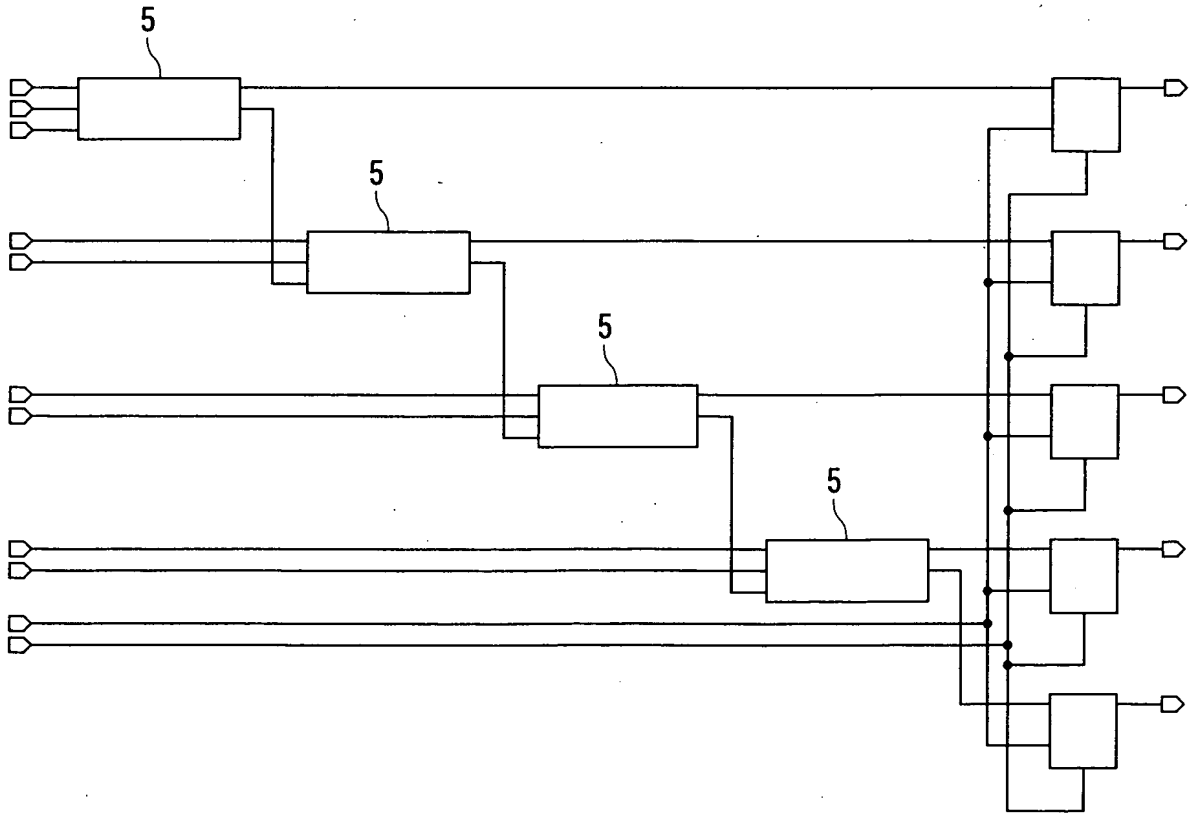
5
5
5
5

FIG. 16